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IN THE CLAIMS:

Please add new claims 33-39 as follows.

1. (Previously Presented) A differential current driver having two output terminals, a common node, a current source connected directly to the common node and supplying a first current to the common node, two switches connected to the common node and to the two output terminals, and a circuit for selectively closing the two switches according to data to be transmitted, the current source having a control terminal receiving a bias signal, the first current being controlled by the bias signal, the differential current driver comprising:

a comparison circuit for receiving the bias signal and mirroring the first current to obtain a second current, comparing the second current with a reference value and generating a control signal having a value responsive to a difference between the second current and the reference value; and

a current adjustment circuit connected to the common node for diverting part of the first current away from the switches responsive to the control signal.

2. (Previously Presented) The differential current driver of claim 1, wherein the current adjustment circuit comprises a transistor for shunting part of the first current to a node different from the two output terminals and the common node.

3. (Previously Presented) The differential current driver of claim 2, wherein the node different from the two output terminals and the common node is a ground node, and the transistor has a source terminal connected to the ground node, a gate terminal receiving the control signal, and a drain terminal connected to the common node.

4.-20. (Canceled)

21. (Previously Presented) A differential current driver comprising:

a first transistor connected directly to a first node, the first transistor having a gate electrode connected to a second node;

a first switch circuit connected to the first node and a first output terminal;

a second switch circuit connected to the first node and a second output terminal;

a controller controlling the first and second switch circuits according to voltage levels of two input signals;

a comparison circuit connected to the second node, for comparing a first current generated by a voltage level of the second node and a reference current and outputting a comparison result; and

an adjustment circuit generating a current path between the first node and ground on the basis of the comparison result.

22. (Previously Presented) The differential current driver of claim 21, wherein the first transistor is a p-channel metal-oxide-semiconductor (PMOS) transistor.

23. (Previously Presented) The differential current driver of claim 22, wherein the first and second switch circuits are PMOS transistors.

24. (Previously Presented) The differential current driver of claim 22, wherein the adjustment circuit is a PMOS transistor.

25. (Previously Presented) The differential current driver of claim 21, wherein the comparison circuit comprises:

a second transistor having a gate electrode connected to the second node;

a reference current source generating the reference current; and

a differential amplifier connected to the second transistor and the reference current source and outputting the comparison result.

26. (Previously Presented) The differential current driver of claim 25, wherein the second transistor is proportional to the first transistor.

27. (Previously Presented) A differential current driver comprising:

a first transistor connected to a first node, the first transistor having a gate electrode connected to a second node;

a first switch circuit connected to the first node and a first output terminal;

a second switch circuit connected to the first node and a second output terminal;

a controller controlling the first and second switch circuits according to voltage levels of two input signals;

a comparison circuit connected to the second node, for comparing a first current generated by a voltage level of the second node and a reference current and outputting a comparison result; said comparison circuit comprising:

a second transistor having a gate electrode connected to the second node, said second transistor being proportional to the first transistor;

a reference current source generating the reference current; and

a differential amplifier connected to the second transistor and the reference current source and outputting the comparison result; and

an adjustment circuit generating a current path between the first node and ground on the basis of the comparison result;

wherein a drain current of the second transistor is smaller than a drain current of the first transistor.

28. (Previously Presented) The differential current driver of claim 27, wherein the second transistor is a PMOS transistor.

29. (Previously Presented) A differential current driver comprising:

a first transistor connected to a first node, the first transistor having a gate electrode connected to a second node;

a first switch circuit connected to the first node and a first output terminal;

a second switch circuit connected to the first node and a second output terminal;

a controller controlling the first and second switch circuits according to voltage levels of two input signals;

a comparison circuit connected to the second node, for comparing a first current generated by a voltage level of the second node and a reference current and outputting a comparison result; said comparison circuit comprising:

a second transistor having a gate electrode connected to the second node;

a reference current source generating the reference current; and

a differential amplifier connected to the second transistor and the reference current source and outputting the comparison result; and

an adjustment circuit generating a current path between the first node and ground on the basis of the comparison result;

wherein the comparison circuit further comprises a current mirror circuit connected to the second transistor and the reference current source.

30. (Previously Presented) The differential current driver of claim 21, wherein the controller comprises:

a first inverter receiving a first signal;

a second inverter connected to the first inverter;

a first NAND circuit connected to the second inverter and the first switch circuit and receiving a second signal; and

a second NAND circuit connected to the first inverter and the second switch circuit and receiving the second signal.

31. (Previously Presented) The differential current driver of claim 30, wherein the first and second switch circuits are PMOS transistors.

32. (Previously Presented) The differential current driver of claim 31, wherein the first NAND circuit is connected to a gate electrode of the first switch circuit, and the second NAND circuit is connected to a gate electrode of the second switch circuit.

33. (NEW) The differential current driver of claim 1, wherein the differential current driver receives a first command signal indicating validity of the data to be output and a second command signal for enabling and disabling the two switches, further comprising a switching circuit for conducting the first current to a first node different from the two output terminals while the first command signal indicates that the data to be output are valid but the second command signal disables the two switches.

34. (NEW) The differential current driver of claim 33, wherein the switching circuit comprises:

a logic gate for performing a logic operation on the first command signal and the second command signal to generate a switch control signal; and

a switch controlled by the switch control signal.

35. (NEW) The differential current driver of claim 34, wherein the first node is a ground node and the switch controlled by the switch control signal is a transistor having a source terminal connected to the first node, a gate terminal receiving the second control signal, and a drain terminal connected to a common node through which the first current passes from the first current source to the two switches.

36. (NEW) The differential current driver of claim 33, wherein the current adjustment circuit comprises a transistor for shunting part of the first current to a second node different from the two output terminals.

37. (NEW) The differential current driver of claim 36, wherein the second node is a ground node, and the transistor has a source terminal connected to the second node, a gate terminal receiving the first control signal, and a drain terminal connected to a common node through which the first current passes from the first current source to the two switches.

38. (NEW) The differential current driver of claim 33, wherein the current source receives a bias voltage controlling the first current, and the comparison circuit comprises:

a comparison current source for generating a second current responsive to the bias voltage, the second current mirroring the first current;

a reference current source for generating a reference current;

a pair of loads for converting the second current to a second voltage and converting the reference current to a third voltage; and

a differential amplifier for generating the first control signal from the second voltage and the third voltage.

39. (NEW) The differential current driver of claim 38, wherein the second current is less than the first current.